REMARKS

Claims 1-15 are presented for examination.

Objections to Drawings

Figure 1 has been objected to for not showing the legend such as Prior Art. Figure 1 has been amended to include the proposed legend.

Claim Objections

Claims 8, 10, and 14 are objected for certain informalities. Claims 8 and 14 have been amended to remove the informalities.

As to claim 10, Applicants do not see any informality. Applicants respectfully request the Examiner to further clarify the objection so the claim can be amended accordingly.

Rejection of Claims under 35 USC §103(a)

Claims 1, 2, and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney et al. (U.S. Patent 5,487,092) in view of Alston (U.S. Patent 6,055,285). Applicants respectfully traverse these rejections.

There are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142. The combination of Finney et al. and Alston do not disclose, teach or suggest each and every limitation of claim 1.

I. The cited references do not suggest or provide motivation to modify or combine their teachings.

The Examiner has state that "It would have been obvious to one with ordinary skill in the art at the time of invention to include the write valid latch and the reset logic for the purpose of not having data mistakenly written into a buffer entry before it has been read out from the buffer." Applicants respectfully disagree.

Finney et al. discloses a system with **two separate buffers**; the external buffer registers 28 and the internal buffer registers 38. Each buffer register is controlled by clocks from different domains. The incoming data is written into the external buffer register 28 using the external clock and then it is transferred to the internal buffer register 38 using the internal clock. The data in the external buffer register 28 is written independently of the condition of the corresponding internal register. Thus, there is no correlation between the write and the read operations except that when the data is ready in the external buffer register 28, the read valid flag 'Rx" is set for the internal register 38 to accept the data. In contrast, Alston discloses a dual-port FIFO where the data is written and read from the same storage element by each clock domain thus, requiring safety logic to prevent the overlap of read and write operation on the same storage element.

Further, in Finney et al., the data in each external buffer register 28 is written using a derivative of the external clock 16 (*see* figure 1, element 30, clock 1-8). Thus, the data is written in each external buffer register using a dedicated clock for each register. In contrast, in Alston, the data in the FIFO buffer memory 110 is written using the same external clock 106, requiring a write enable signal for each memory location.

Therefore, not only it would not have been obvious to one skilled in art to combine the disclosures of Finney et al., and Alston, but in fact, Finney et al. and Alston teach away from each other because of different buffer structures. Accordingly, Finney et al. and Alston do not suggest or provide motivation to combine their disclosures and claim 1 is patentably distinguishable from the cited references.

II. The combination of Finney et al. and Alston do not show, teach or suggest all the claim limitations.

As to the read valid latch, the Examiner has stated that Finney et al. shows "a read valid latch for controlling the state of a valid line in the transmit clock domain, the read valid latch having a reset input coupled **to receive a read request signal** (figure 3, element 48 it should be noted that although figure 3 does not show the latch having a reset input, it is well known in the art that latches of all kinds have reset inputs on them)..." (Emphasis added) Applicants respectfully disagree.

First, the cited element 48 is not a "read valid latch" instead it is an intermediate latch in the sampling circuit 36 (*see* figure 3). Second, the element 48 is not part of the transmit clock domain, instead it is part of the receive clock domain and receives the derivative clock 1 of the external clock 16 (*see* figure 3, elements 32 and 48, left side of the asynchronous boundary). Third, Finney et al. does not show a read request signal because the data from the internal buffer register 38 is read by the Multiplexer 40 in a round-robin sequence (*see* col. 7, lines 26-32). Thus, Finney et al. does not even need a read request signal as recited in claim 1.

As to the set logic for setting the read valid latch, the Examiner has stated that Finney et al. shows "set logic for setting the read valid latch **responsive to the write request signal** (col. 5, lines 56-61 and figure 3, where the signal from element 46 into valid latch 48 indicates the data is read [sic] to be written into the appropriate entry in buffer 38,)." (Emphasis Added) Applicants respectfully disagree.

Contrary to the Examiner's assertion, Finney et al. do not show a write request signal. Further, the data from the output data bus and the boundary register 24 has already been written into the external buffer registers 28 before the data is actually transferred to the internal buffer register 38. The signal identified by the Examiner is in fact an intermediate signal for the latch 48 in combination of two different clock periods, Phase 1 and clock 1, that provides metastability for each element. Thus, Finney et al., does not show a combination of a write request signal and a set logic as recited in claim 1.

As to the write valid logic and reset logic, the Examiner has cited the ACK signal from the write controller 140 in Alston. The cited sections in Alston refer to a situation where the write address pointer points to a memory location that has not been read. The write controller 140 detects the collision of read/write address pointers and inhibits ACK signal until the data from the corresponding location is read by the receiving circuit. The write controller 140 does not respond to a read request signal as recited in claim 1 instead, the write controller 140 independently determines the collision of the write and read addresses by comparing each address, regardless of the read operation (*see* col. 7, lines 44-63). In Alston, the write controller 140 and the read controller 142 independently perform corresponding operations and each read/write operation is executed independently. Thus, Alston does not show a reset logic for resetting the write valid latch **responsive to the read request signal** as recited in claim 1.

III. The combination of Finney et al. and Alston does not provide the reasonable expectation of success.

As explained above, Finney et al. discloses a system with two individual buffer registers where Alston describes a system with a dual-port FIFO. The controls shown in Alston are configured for simultaneous read/write operation from the same memory in a first-in-first-out manner. A reasonable person skilled in art will not combine a dual-port memory control circuit with a bank of individual buffer register, which is designed for a round-robin write sequence operation. Further, the combination of Alston and Finney et al. will not work because first, Finney et al. requires discarding "pad words" in the incoming data and adding additional "pad words" in the output data (*see* col. 5, lines 10-26). Second, Finney et al. requires register-resequencing to reassemble the data in proper sequence before the data is read by the receiving circuit (*see* col. 5, line 66 – col. 6, line 5). The individual buffer register structure of Finney et al. allows the multiplexer 40 to reassemble the data before the data is outputted on the bus 18. In contrast, Alston discloses a first-in-first-out buffer in which the data is read in the order that it was written in. Therefore, no reasonable person skilled in art will combine the fixed data sequence of Alston with the re-sequencing of Finney et al. Accordingly, the combination of

Finney et al. and Alston does not provide the reasonable expectation of success and claim 1 is patentably distinguishable from the combination of cited references.

Claim 2 depends from claim 1 and is patentably distinguishable from the combination of cited references for at least the same reasons as claim 1. Further, the Examiner has cited the write pointer 122 and the read pointer 132 of Alston in combination of the structure in Finney et al. and has stated that "It would have been obvious to one with ordinary skill in the art at the time of invention to **include the pointers with the interface of claim 1** for the same reasons and motivation as in claim 1." (Emphasis added). Applications respectfully disagree.

Applicants would like to point to the Examiner that Finney et al. discloses a buffer register bank in which the data is written in round-robin sequence order using various derivatives of the external clock 16 (*see* figure 1, elements 28, 16, and 30). Further, Finney et al. requires re-sequencing of data at the output. In contrast, the read/write pointers of Alston do not allow re-sequencing of corresponding memory locations as required by Finney et al. "The proposed modification cannot render the prior art unsatisfactory for its intended purpose." *See* M.P.E.P. §2143.01. Accordingly, claim 2 is further patentably distinguishable from the combination of cited references.

Regarding claim 5, Applicants would like to respectfully point to the Examiner that Finney et al. discloses two independent banks of buffer register and the read/write valid bits are not associated with the same first one of the plurality of entries as recited in claim 1. Further, Finney et al. does not show read and write valid bits for each register as recited in claim 5 instead Finney et al. discloses a separate bank of register for each of the write and read operation.

Further, the Examiner has cited read/write pointers of Alston in the manner of claim 1. As explained above, Finney et al. discloses a buffer register bank in which the data is written in a round-robin sequence order using various derivatives of the external clock 16 (*see* figure 1, elements 28, 16, and 30). Furthermore, Finney et al. requires re-sequencing of data at the output and the read/write pointers of Alston do not allow re-sequencing of corresponding memory locations are required by Finney et al. Thus, it would not have been obvious to one with ordinary skill in the art at the time of invention to include write/read pointers of Alston in the structure of

Finney et al. Accordingly, claim 5 is patentably distinguishable from the combination of cited references.

Claim 6 depends from claim 5 and is patentably distinguishable form the combination of cited reference for at least the same reasons as claim 5. Further, as explained above, Finney at al. stores data in round-robin sequence using various derivatives of the external clock 16 and requires re-sequencing of registers at the output. In Finney et al., each external register 28 receives its own dedicated clock (*see* figure 1, element 30, and clock 1-8). Thus, Finney et al. does not require write/read pointers such as shown in Alston. In fact, the individual clock structure of Finney et al. teaches away from using read/pointers. Accordingly, claim 6 is further patentably distinguishable form the combination of the cited references.

Claim 7 depends from claim 5 and is patentably distinguishable form the combination of cited reference for at least the same reasons as claim 5. Further, as explained above, Finney et al. re-sequences the data at the output bus 18 using the multiplexer 40. Thus, the read pointer is not even needed because the outputs of all the internal buffer registers 38 are available to the multiplexer 40 for proper re-sequencing. Therefore, Finney et al. cannot be combined with Alston. In fact, Finney et al. teaches away from using a read pointer. Accordingly, claim 7 is further patentably distinguishable from the combination of the cited references.

Claim 9 depends from claim 5 and is patentably distinguishable form the combination of cited reference for at least the same reasons as claim 5.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Finney et al. and Alston as applied to claim 1 above, and further in view of Cassiday et al. (U.S. Patent 5,799,175). Applicants respectfully traverse these rejections.

Claim 3 depends from claim 1 and is patentably distinguishable from the combination of Finney et al. and Alston for at least the same reasons as claim 1. Thus, the combination of Finney et al. and Alston with Cassiday cannot render claim 3 obvious.

Further, the combination of various independent elements of each of the references does not work as the Examiner has suggested. For example, the Examiner has combined an edge detector 72 of Cassiday et al. with the synchronization circuits 210 and 212 of Alston. Applicants would like to respectfully point to the Examiner that the synchronization circuits 210 and 212 of Alston are configured to avoid the kind of problems generated by the edge transition detection of each address pointer. According to Alston, the synchronization circuits 210 and 210 are configured to assure that the read/write address pointers are stable before the corresponding controller evaluates these pointers (*please see* col. 8, line 11 – col. 9, line 16, and figures 3 and 5). Thus, Alston actually teaches away from using edge transition detection of the read/write pointers and therefore, the edge detector 72 of Cassiday et al. cannot be combined with the synchronization circuits 210 and 210 of Alston. Accordingly, claim 3 is further patentably distinguishable form the combination of the cited references.

Claim 4 depends from claim 1 and is patentably distinguishable from the combination of Finney et al. and Alston for at least the same reasons as claim 1. Thus, the combination of Finney et al. and Alston with Cassiday cannot render claim 4 obvious. Further, as explained above, the edge detector of Cassiday et al. cannot be combined with the synchronization circuits of Alston because the combination renders the synchronization circuits inoperable for its intended purpose. Accordingly, claim 4 is further patentably distinguishable form the combination of the cited references.

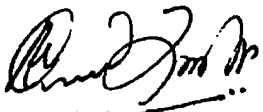
Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lowe et al. (U.S. Patent 6,233,221 131) in view of Finney et al. in further view of Alston. Applicants respectfully traverse these rejections.

As to claim 10, Lowe et al. do not disclose the internal structure of each of the switching elements. The structural elements of claim 10 have been rejected in the manner of claim 1, which has been distinguished from the combination of Finney et al. and Alston for failing to disclose each and every element of claim 1. Accordingly, claim 10 is patentably distinguishable from the combination of the cited references for at least the same reasons as claim 1.

Claims 11-13 and 15 depend from claim 10 and are patentably distinguishable from the combination of the cited references for at least he same reasons as claim 10.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, the Examiner is requested to please contact the below named attorney for Applicants.

Respectfully submitted,



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